DRIVVEN

A National Instruments Company

AD Combo Module Kit User's Manual

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Contents

Introduction 3
Pinout 4
Hardware 5
Powering the Module 5
Platform Compatibility 6
Analog Inputs 8
  Standard Channel Configuration 8
    Generic Analog Input Circuit 8
    Divided Inputs 9
    Active Inputs / Potentiometer Inputs 10
    Thermistor Inputs / Switch Inputs 11
VR Sensor Inputs 12
Hall-Effect Sensor Inputs 15
Software Installer 16
Creating a LabVIEW Project 17
Sub VI Documentation 19
Examples 22
Standard Circuit Configuration 23
Custom Configuration 24
Compliance and Certifications 26
Physical Specifications and Characteristics 27

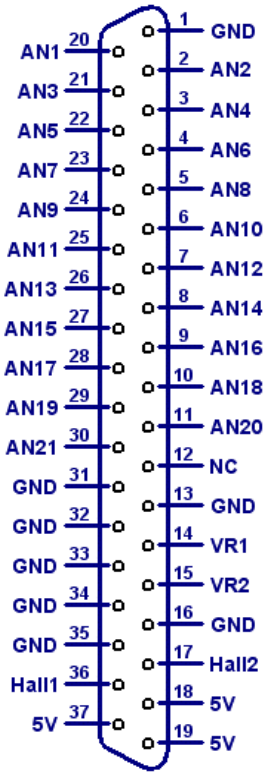
Introduction

The Drivven cRIO AD Combo Module Kit offers a set of automotive-style analog and digital inputs to interface with standard automotive sensors.

Features:

- 21 Ch. Analog inputs
  - 12-bit A/D Converter
  - 4 ksps per channel
  - Optional pullup, pulldown, and divide resistors (manually configurable)
  - Anti-aliasing filter per channel
  - Dedicated 2.5V precision reference
- 2 Ch. VR sensor inputs
  - 60VDC input range
  - Adaptive arming threshold
- 2 Ch. Hall-effect sensor or general purpose digital inputs
  - Digital input with inverting Schmitt trigger hysteresis
  - Short circuit protection
  - Optional pullup, pulldown, and divide resistors
  - Analog filter for noise rejection
- Sensor power output at DB37 connector (pins 18, 19 & 37)
  - 5V @ 100mA

Pinout


1 GND
2 AN2
3 AN4
4 AN6
5 AN8
6 AN10
7 AN12
8 AN14
9 AN16
10 AN18
11 AN20
12 NC
13 GND
14 VR1
15 VR2
16 GND
17 Hall2
18 5V
19 5V
20 AN1
21 AN3
22 AN5
23 AN7
24 AN9
25 AN11
26 AN13
27 AN15
28 AN17
29 AN19
30 AN21
31 GND
32 GND
33 GND
34 GND
35 GND
36 Hall1
37 5V

Hardware

This module provides analog inputs, VR sensor inputs and hall-effect sensor inputs. It also provides sensor power and ground. Sensor power is provided directly from the cRIO chassis backplane. Sensors should not draw more than a total of 100mA.

A properly strain relieved DB-37 connector (not included) is used to interface to the module. National Instruments provides the "cRIO-9933 37-pin Conn. Kit, screw term conn. and DSUB shell" which is compatible with this module. However, any DB-37 connector system may be used. Drivven recommends the following DB-37 connector parts and tools available from several electronics parts distributors (Allied, Mouser, Digikey, etc.).

Table 1. Connector parts list

Description	Mfr.'s Part #
AMP HDP-20 Series 109 37P Receptacle Housing	1757820-4
AMP HDP-20 Series 109 Crimp Socket Contact	205090-1
Norcomp D-Sub Connector Hood, 37P 45 Degree	971-037-020R121
AMP D-Sub Insert/Extract Tool	91067-2
Paladin D-Sub 4-Indent Crimp Tool 26-20 AWG	1440

Powering the Module

The AD Combo module requires power from one source, from the CompactRIO backplane male high density D-Sub 15-pin (HD15) connector which mates with the module's female HD15 connector. This power source provides a regulated 5 volts and ground to various digital logic and analog functions within the module. The CompactRIO 5V source is active whenever the CompactRIO or R-Series Expansion Chassis is properly powered. The module should only be powered at the HD15 connector by plugging it into a CompactRIO or R-Series Expansion Chassis. The module's HD15 connector should not be connected to any other device. **Do not** connect 5VDC power to the "5V" outputs of the DB37 connector. Those pins are 5V outputs.

Platform Compatibility

CompactRIO modules from Drivven are compatible within two different platforms from National Instruments. One platform is CompactRIO, consisting of a CompactRIO controller and CompactRIO chassis as shown in Figure 1a below.

Figure 1a. CompactRIO platform compatible with Drivven CompactRIO modules.

The other platform is National Instruments PXI which consists of any National Instruments PXI chassis along with a PXI RT controller and PXI-78xxR R-Series FPGA card. An R-Series expansion chassis must be connected to the PXI FPGA card via a SHC68-68-RDIO cable. The CompactRIO modules insert into the R-Series expansion chassis. This platform is shown in Figure 1b below.

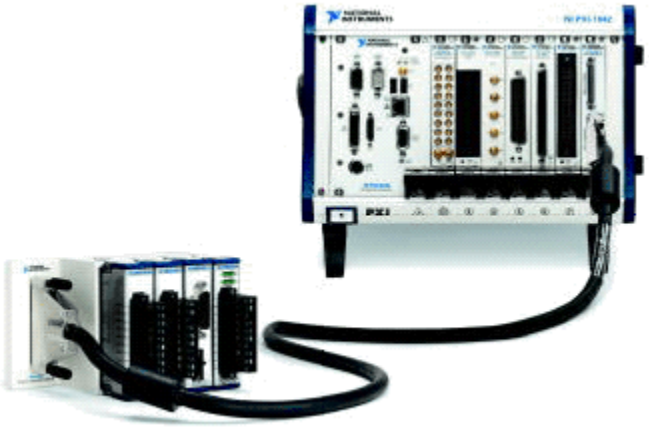


Figure 1b. PXI platform compatible with Drivven CompactRIO modules.

Drivven CompactRIO modules are not compatible with the National Instruments CompactDAQ chassis.

Drivven CompactRIO modules REQUIRE one of the hardware support systems described above in order to function. The modules may not be used by themselves and/or interfaced to third party devices at the backplane HD15 connector. These efforts cannot be supported by Drivven or National Instruments.

You can use Drivven C Series modules with NI cRIO-911x, NI cRIO-907x, and NI R Series Expansion systems under the following conditions.

–Leave one empty chassis slot between Drivven and NI modules.
–Maintain an ambient system operating temperature of 0 to 45 °C.
–Typical specifications of NI modules may not apply when used in a system with Drivven modules.
–Warranted specifications are guaranteed for all NI modules except thermocouple modules when used in a system with Drivven modules.
–The NI 9214 is recommended for thermocouple measurements in cRIO systems using Drivven modules.
–Scan Interface mode, auto-detection, and ID mode are not supported for Drivven modules.

Analog Inputs

All analog inputs are similar to production automotive ECU analog inputs. They are single ended inputs and provide filtering and over/under voltage protection.
For best results, the power and ground of the sensors should be provided by this module.
A pullup or pulldown is recommended for every input in order to facilitate open/defective sensor faults. These are provided with the standard configuration.

Standard Channel Configuration

Generic Analog Input Circuit

Figure 2 shows the generic schematic representation of all analog inputs. An AD Combo module having a standard configuration will have a mixture of channel configurations according to the circuits described below.

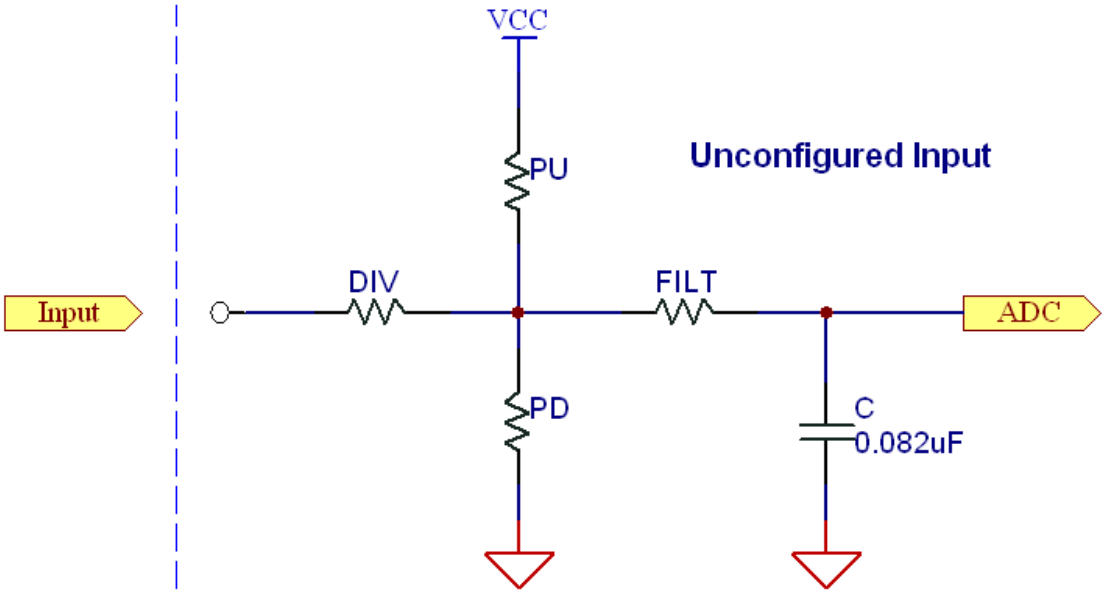


Figure 2. Unconfigured generic analog input circuit schematic

Divided Inputs

Figure 3 shows the analog input circuit configuration for measuring voltages from 0 to 33 V. This is standard configuration for channels 1 - 3. Channels with this configuration are protected from voltage swings of +/-50V.

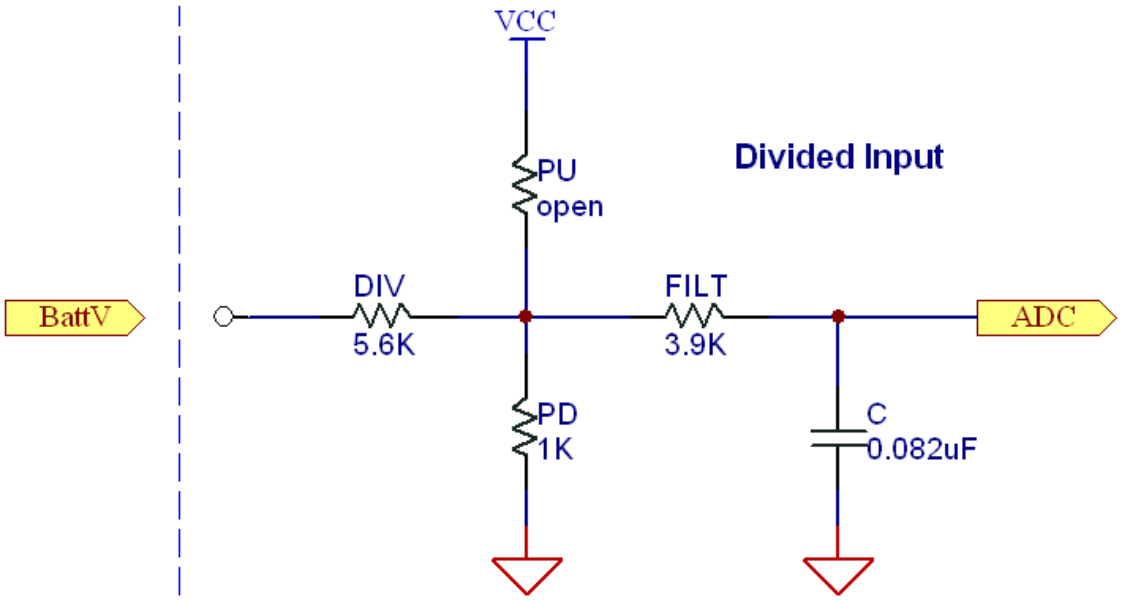


Figure 3. Analog input configuration for 0 to 33 V inputs.

Active Inputs / Potentiometer Inputs

Figure 4 shows the analog input circuit configuration for both active-drive analog sensors and potentiometers for measuring voltages from 0 to 5 V. This is the standard configuration for channels 4 - 16. Channels with this configuration are protected from voltage swings of +/-30V.

This circuit utilizes a weak pulldown for open circuit detection. If the channel is connected to a potentiometer, the pulldown will slightly modify the voltage seen by the A/D converter, as compared to an input circuit without the pulldown. Therefore, a full potentiometer calibration must be performed since the voltage from this circuit will not readily correlate to the voltage resulting from no pulldown.

Examples of potentiometers are throttle position and pedal position sensors.

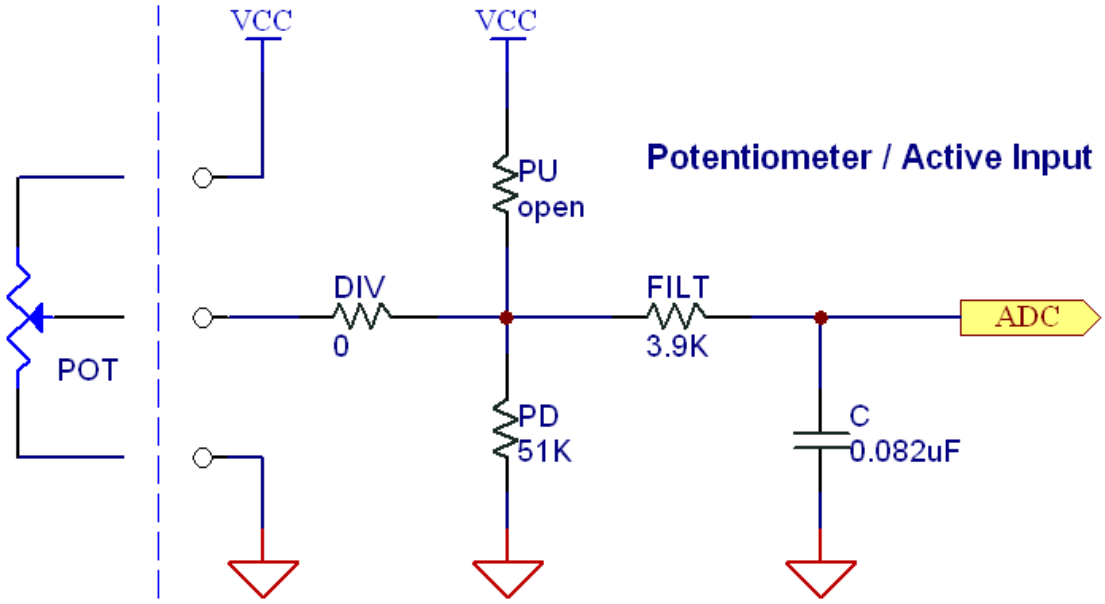


Figure 4. Analog input configuration for active sensors and potentiometers

Thermistor Inputs / Switch Inputs

Figure 5 shows the analog input circuit configuration for thermistors and switches, for measuring voltages from 0 to 5 V. This is standard configuration for channels 17 - 21. Channels with this configuration are protected from voltage swings of +/-30V.

Thermistor inputs have a strong pullup to create a voltage divider with the sensor. Refer to the sensor datasheet for sensor resistance curves. Most production automotive temperature sensors are thermistors which have a maximum cold resistance of approximately 100 Kohms and a resistance of approximately 100 ohms at 150 degrees C. The pullup resistor of 1 Kohms will provide a useable output voltage range for thermistors of this type.

When used as a switch input, the switch should short to ground when it is closed.

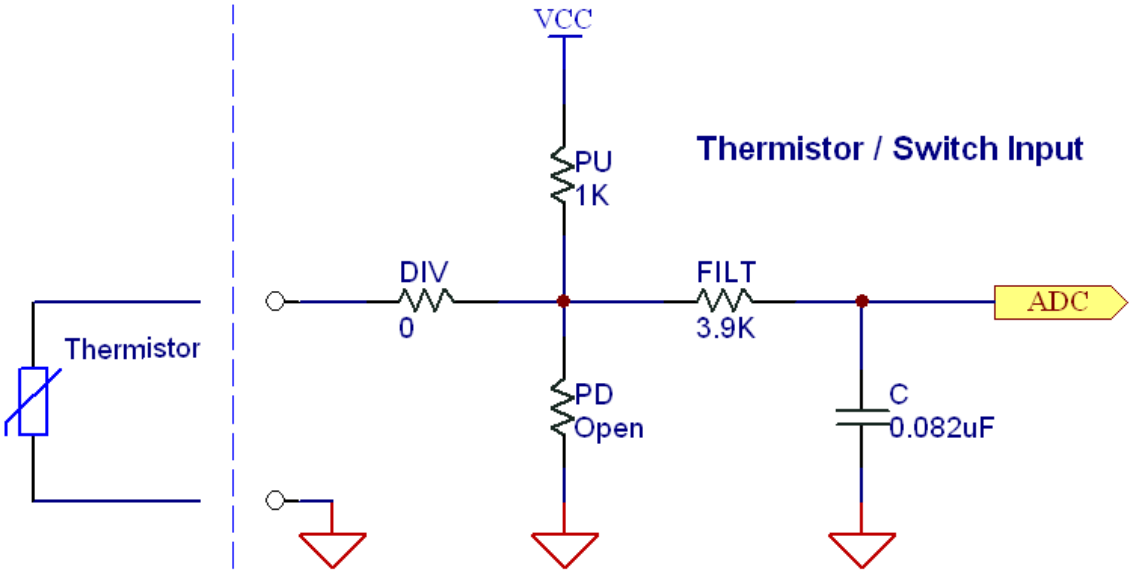


Figure 5. Analog input configuration for thermistors and switches

VR Sensor Inputs

The AD Combo module provides two identical VR sensor inputs. A Variable Reluctance (VR) sensor input is a standard low cost automotive speed sensing input. It is an electro-magnetic sensing device containing a winding of wire around a permanent magnetic core. It relies on the movement of ferrous material (steel teeth) past the tip of the sensor to change the magnetic flux of the sensor. This creates a voltage pulse across the leads of the sensor's wire coil. Figures 8 and 9 below show a typical VR signal with respect to toothed wheels, as shown in Figures 6 and 7. The VR signal will go positive as a tooth approaches the sensor tip. The signal will then rapidly swing back through zero precisely at the center of the tooth. As the tooth moves away from the sensor tip the voltage will continue in the negative direction and then return to zero.

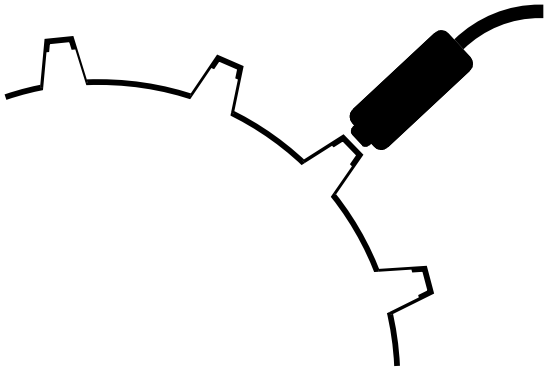


Figure 6. Positive tooth trigger wheel

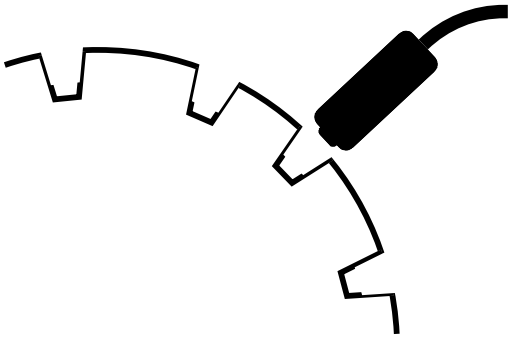


Figure 7. Negative tooth trigger wheel

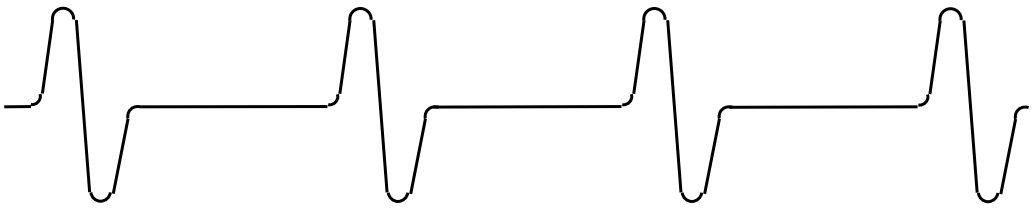


Figure 8. Correct signal polarity for VR input circuit

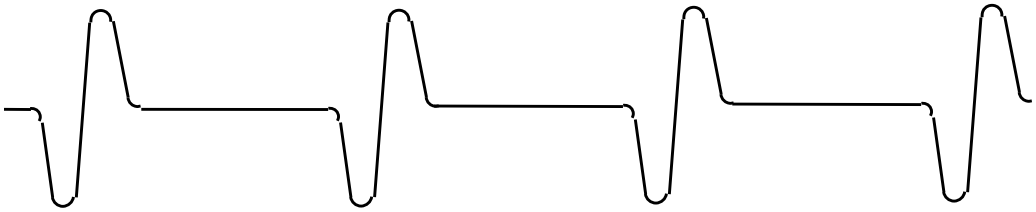


Figure 9. Incorrect signal polarity for VR input circuit

Each VR sensor input requires two connections. The AD Combo module pins labeled VR1 and VR2 are the positive sensor inputs. The negative sensor inputs must be connected to GND pins on the module. The polarity of the sensor connection to the module is critical. The leads of the sensor should be connected such that the positive input of the VR circuit sees the waveform shown in Figure 8. The waveform shown Figure 9 is incorrect, and the VR circuit will not properly respond to this waveform. The rapid zero crossing of the VR signal must be in the negative direction.

The polarity of the physical tooth or gap on the trigger wheel will contribute to the polarity of the voltage pulse from the sensor. Figure 6 demonstrates a positive physical tooth polarity and Figure 7 demonstrates a negative physical tooth polarity. Assuming the lead polarity of a sensor remained the same, one of the configurations would generate the waveform shown in Figure 8, while the other configuration would generate the waveform shown in Figure 9.

Triggers wheels are designed so that the physical center of each tooth or gap corresponds to a known angular position of the wheel. This physical center of the tooth or gap always corresponds to the rapid zero-crossing of the generated voltage pulse.

The VR circuit is designed so that the rapid negative zero-crossing of the raw sensor signal corresponds to the rising edge of a digital pulse sent to the RIO FPGA. The VR output signal to the FPGA will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. An example of this is shown in Figure 10. Within LabVIEW FPGA the system designer can route this digital signal to the EPT CrankSig or CamSig input. The signal can also be routed to any other speed measurement sub-VI.

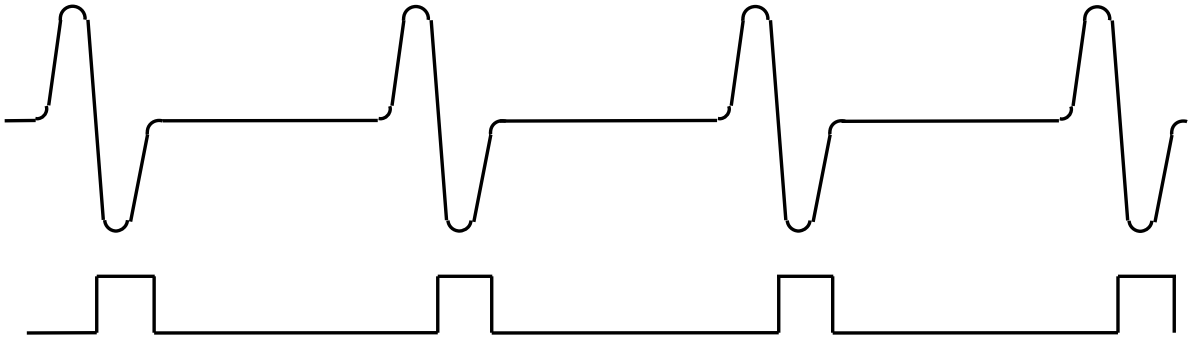


Figure 10. VR input pulse and resulting digital output from VR circuit

The absolute maximum VR pulse amplitude allowed by the circuit is 60VDC. If the input signal exceeds this voltage, damage may occur to the circuit. The amplitude should not exceed 60VDC at maximum engine speed. The minimum VR pulse amplitude that will generate a digital output by the VR circuit is +/-200 millivolts.

The VR circuit implements adaptive noise rejection features during continuous incoming VR pulses. In general, an adaptive arming threshold voltage is generated with each VR pulse and bleeds down thereafter. The next pulse must have an amplitude that exceeds the arming threshold in order for a digital output to be generated at the rapid zero-crossing. The initial arming threshold is set to approximately 70% of each pulse's amplitude.

Given a constant gap between the sensor and the trigger teeth, the amplitude of a VR pulse is directly proportional to the speed of the trigger wheel. For example, if the VR amplitude at 1000 RPM is +/-10 volts, then the amplitude at 2000 RPM will be +/-20 volts. By using an oscilloscope to measure the VR amplitude at a low speed, this relationship can be used to determine what the maximum amplitude will be at the maximum speed. If the maximum amplitude of 60VDC will be exceeded at maximum speed, then the sensor gap must be increased, or the designer must obtain a custom VR circuit configuration from Drivven.

Hall-Effect Sensor Inputs

The AD Combo module provides two identical hall-effect sensor input circuits. The hall-effect inputs are designed to take a digital input from a hall-effect or proximity sensor. Typical sensors of this type will have an open-collector output, requiring a pullup resistor at the collector. The hall-effect inputs will also read active TTL compatible signals. The standard configuration includes a 4.7K pullup to 5V for use with open collector type inputs. The input is protected against typical automotive battery voltages and can be connected to actively-driven, battery voltage signals. Channels with this configuration are protected from voltage swings of +/-30V.

The circuit's output to the RIO FPGA reverses the polarity of the input by going low when the input voltage is greater than 2.0V. The output goes high when the input is less than 1.0V.

Figure 11 shows the standard configuration of the hall-effect sensor input circuits.

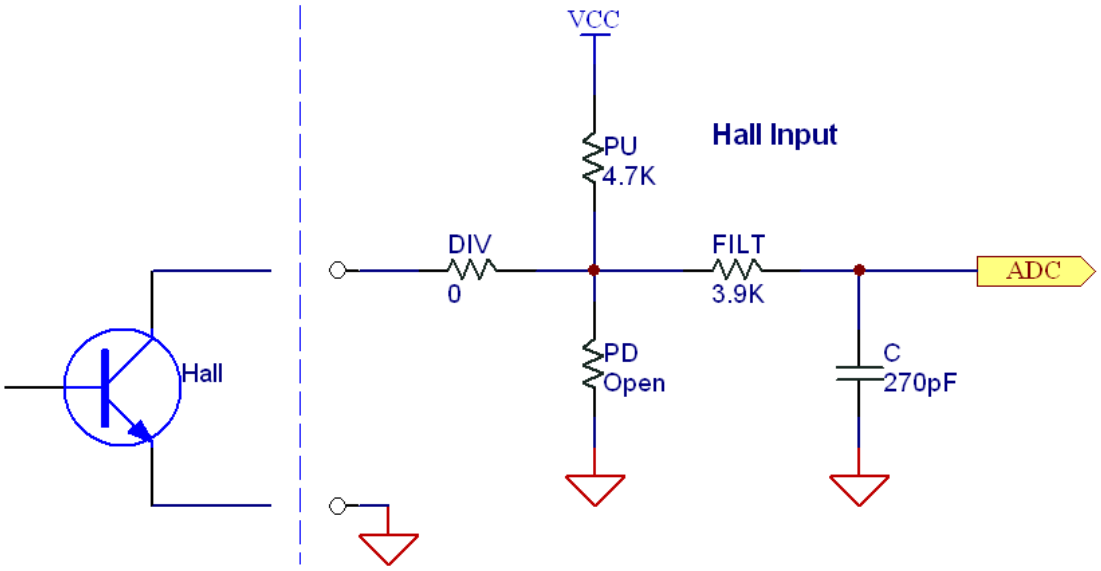


Figure 11. Hall-effect circuit input configuration

Software Installer

The AD Combo Module Kit is provided with an installer package which may be downloaded from Drivven's Sharepoint website after obtaining login access from Drivven. User's may go to http://portal.drivven.com/SoftwareDownload and enter the provided username and password to gain access to the specific product installer packages which have been purchased. The installer packages are executables which should be run on the intended development computer, having LabVIEW development tools installed. After installing the package, a "Start->Programs->Drivven->ProductRelease" menu item will be added to the desktop. The specific product will have an example LabVIEW project appear under the "Examples" menu and the user manual will appear under the "Manuals" menu. User's may copy and open the example project to experiment with the module or use as a starting point for a new application. All software files, example projects and documentation are installed to:

C:\Program Files\National Instruments\LabVIEW X.X\vi.lib\addons\DrivvenProductRelease\.

When working with block diagrams, user's will notice a "Drivven" function palette added to the standard LabVIEW palette, specific for the RT or FPGA target. VIs for a specific Drivven product will be categorized according to product name. Also, some Drivven products will install RT and FPGA VIs under a "General" function palette which is intended to be used across multiple products.

Requirements
The Drivven VIs require:

- LabVIEW 8.5 Full Development or later
- LabVIEW RT Module 8.5 or later
- LabVIEW FPGA Module 8.5 or later
- NI-RIO 2.4 or later

The AD Combo Module Kit is provided with a LabVIEW FPGA VI for interfacing with the module and providing the analog-to-digital conversion results for each analog input channel. The unsigned 16-bit integer results may be used within the FPGA or read by RT controller for conversion to engineering units. The digital signals from the VR and Hall inputs are also provided and may be wired to any other function within the FPGA. Figure 12 shows the icon which represents the supplied FPGA VI.

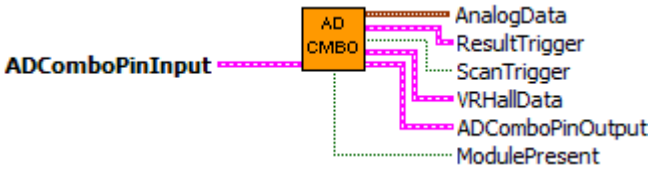


Figure 12. AD Combo VI icon with leads.

The FPGA VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram. The SCL must execute at the default clock rate of 40 MHz.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Creating a LabVIEW Project

Drivven recommends working from the provided example application as a starting point for learning the use of the Drivven software blocks. However, the following section describes starting a LabVIEW project from scratch and adding a Drivven module.

1.) Install the Drivven software by running the installer executable and accepting the software license agreement.
2.) Restart LabVIEW, if previously running, and create a new LabVIEW project.
3.) Give the new project a name by clicking the "Save Project" button on the project toolbar.
4.) Right click on the highest item in the project hierarchy ("Project:…") and navigate to "New->Targets and Devices…"
5.) Within the "Add Targets and Devices…" dialog, select the appropriate radio button, depending on whether you already have an existing powered and configured RT target on the network or if you are adding a new RT target which is not present yet on the network.
    a. Existing Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see the discovered targets in that category.
        ii. Double-click the desired target to add it to your project.
    b. New Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see all possible targets within that category.
        ii. Double-click the desired target to add it to your project.
6.) If the new RT target is not currently on the network, right-click on the RT target within the project and open the properties dialog to set the IP address or DNS name if necessary.
7.) Right-click on the RT target within the project and navigate to "New->Targets and Devices…"
8.) Within the "Add Targets and Devices…" dialog, select the appropriate radio button, depending on whether you already have an existing FPGA target connected to an existing RT target or if you are adding a new FPGA target which is not present yet.
    a. Existing Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see the discovered FPGA targets in that category.
        ii. Double-click the desired target to add it to your project.
    b. New Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see all possible targets within that category
        ii. Double-click the desired target to add it to your project.
9.) If the new FPGA target was not currently in the system, right-click on the FPGA target within the project and open the properties dialog to set the resource name if necessary. The resource name can be found from MAX when connected to the actual remote system.
10.) If the FPGA target is a PXI or PCI card, then a R Series expansion chassis must be added under the FPGA target. This is done by right-clicking on the FPGA target and navigating to "New->R Series Expansion Chassis". Within the following dialog, select the appropriate FPGA connector to which the chassis will be connected. A unique name for the chassis may also be specified.
11.) Right click on the R-Series expansion chassis or cRIO FPGA target chassis and navigate to "New->C Series Modules…"
12.) Select the "New Target or Device" radio button and double-click on the "C Series Module" in the "Targets and Devices" list. In the following dialog, select the desired Drivven module at the bottom of the "Module Type" list. The Drivven modules will be appended there if any Drivven module software has been installed. Select the appropriate module

location. Finally, specify an appropriate name for the module, which will later appear in the FPGA I/O nodes in the FPGA block diagram. Having meaningful module names is important for preventing coding mistakes.

13.) After adding a module to the project, a folder will automatically be added to the project having the same module name given in the module configuration dialog. The folder will contain the FPGA I/O pins for the module slot. These I/O pins can be selected in the block diagram when connecting the module VI PinInput and PinOutput clusters to FPGA I/O nodes. The example application, discussed below, should be consulted for further details about connecting the PinInput and PinOutput clusters to FPGA I/O nodes. Within the example projects, notice the FPGA I/O node elements having module name prefixes.

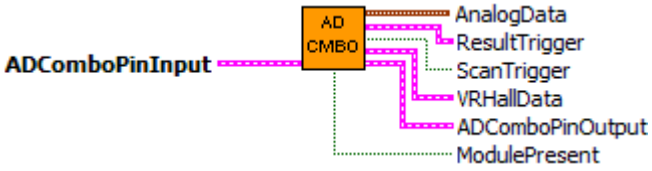
14.) Some Drivven modules can be automatically recognized by LabVIEW when adding cRIO modules to the project. However, Drivven does not recommend using this feature because the module names, which are automatically assigned, are not meaningful (Mod1, Mod2, etc) and can lead to coding mistakes when wiring the Drivven FPGA VIs to the I/O nodes. Adding the modules to the project manually, as described above, is still the recommended method.

Sub VI Documentation

ad_combo_reve.vi

The AD Combo FPGA VI interfaces to the AD Combo module via the PinInput and PinOutput clusters. The VI provides analog, VR and Hall sensor results.

Connector Pane



Controls and Indicators

ADComboPinInput These boolean controls must be connected to their corresponding FPGA I/O Node input item.

ADComboPinOutput The boolean indicator named IDSelectEn must be connected to a Set Output Enable method of an FPGA I/O Method Node. The boolean indicator named IDSelectOut must be connected to a Set Output Data method of an FPGA I/O Method Node. The remaining boolean indicators must be connected to their corresponding FPGA I/O Node output item.

AnalogData The analog to digital conversion results for channels 1-21 and VRef in terms of 12-bit A/D counts from 0 to 4095, corresponding to 0 to 5V.

- **Result_X** The analog to digital conversion results for channels 1-21 in terms of 12-bit A/D counts from 0 to 4095, corresponding to 0 to 5V.
- **VRef (2.5V, 0.2%)** The AD Combo uses a high reference of 5.0V +/-2% for its A/D converters. One channel of the AD Combo measures an analog reference of 2.5V +/-0.2%. The reference value can be used to correct other channels when it is necessary to have a more precise absolute voltage measurement. For channels which are measuring ratiometric signals, such as potentiometers, this correction is not necessary.

VRHallData Cluster of VR and Hall sensor signals

- **VR1** The VR signal will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. It is important to only use the rising edge of this digital signal because it is always lined up with the rapid negative zero crossing of the external VR pulse.
- **VR2** The VR signal will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. It is important to only use the rising edge of this digital signal because it is always lined up with the rapid negative zero crossing of the external VR pulse.
- **Hall1** The Hall signal is an inverted and filtered version of the external signal presented to the hall-effect input channel.

Hall2 The Hall signal is an inverted and filtered version of the external signal presented to the hall-effect input channel.

ResultTrigger A 40 MHz one-clock one-shot output indicating that the associated channels have a new result ready. These signals may be used to trigger algorithms to execute code when new analog results are ready.

ScanTrigger A 40 MHz one-clock one-shot output indicating that all channel registers have been updated once. ScanComplete one-shot will be asserted at the rate of 4000 Hz.

ModulePresent Indicates that the module is connected and recognized by the Drivven software.

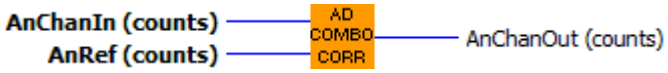
ad_combo_corr.vi

The AD Combo uses a high reference of 5.0V +/-2% for it A/D converters. One channel of the AD Combo measures a reference of 2.5V +/-0.2%. The reference value can be used here to correct other channels when it is necessary to have a more precise absolute voltage measurement. For channels which are measuring ratiometric signals, this correction is not needed.

The A/D counts of AD Combo channel "VRef" should be wired to the AnRef (counts) input.
The A/D counts of the channel to be corrected should be connected to the AnChanIn (counts) input.
The absolute, corrected A/D counts are output on AnChanOut (counts).

Note: This calculation assumes a 12-bit A/D converter and a nominal reference of 2.5V.
Note: This VI should be instantiated at the Windows or RT level, not within the FPGA.

Connector Pane



Controls and Indicators

AnChanIn (counts) A/D result from the AD Combo FPGA VI Result_X indicator.

AnRef (counts) A/D result from the AD Combo FPGA VI VRef (2.5V, 0.2%) indicator.

AnChanOut (counts) Corrected A/D result.

Warning About FPGA I/O Node Wiring

Great care should be taken to ensure that I/O nodes are wired to the correct PinInput and PinOutput clusters of the correct module VI. If wired incorrectly, then undefined behavior or module damage could result. LabVIEW FPGA does not yet provide a method for 3rd party module vendors to hide the DIO pins behind module VIs and still be portable to various system configurations. Therefore, a double-check of the I/O node wiring is recommended.

Two LabVIEW FPGA code snippets are shown below from an ADCombo implementation which illustrate this issue. Figure 13 shows the correct implementation of the FPGA I/O node block for the PinOutput cluster of the ADCombo. On the other hand, figure 14 shows a coding mistake that should be avoided. Notice the ADCombo output items where a Spark module output item is selected instead of the correct ADCombo module output item. This means that the Spark (DIO5) output is being driven by the ADCombo logic and will cause strange behavior of the spark module, or possible damage.

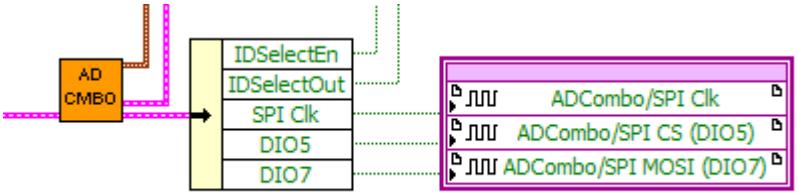


Figure 13. Representative FPGA output node for ADCombo with correct output item selection.

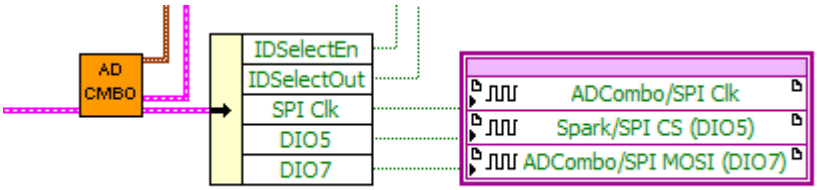


Figure 14. Representative FPGA output node for ADCombo with incorrect output item selection for DIO5. This will cause strange behavior or damage to the spark module. Applying meaningful names to the modules within the project can help identify these coding mistakes.

Examples

The following screen capture in Figure 15 from the example project shows a LabVIEW FPGA block diagram with the AD Combo VI used for general purpose analog and speed measurement. This FPGA application is entirely contained within a single cycle loop, clocked at the required 40 MHz. The PinInput and PinOutput clusters are wired to LabVIEW FPGA I/O pins which are configured for a cRIO controller chassis or a cRIO R-Series expansion chassis.

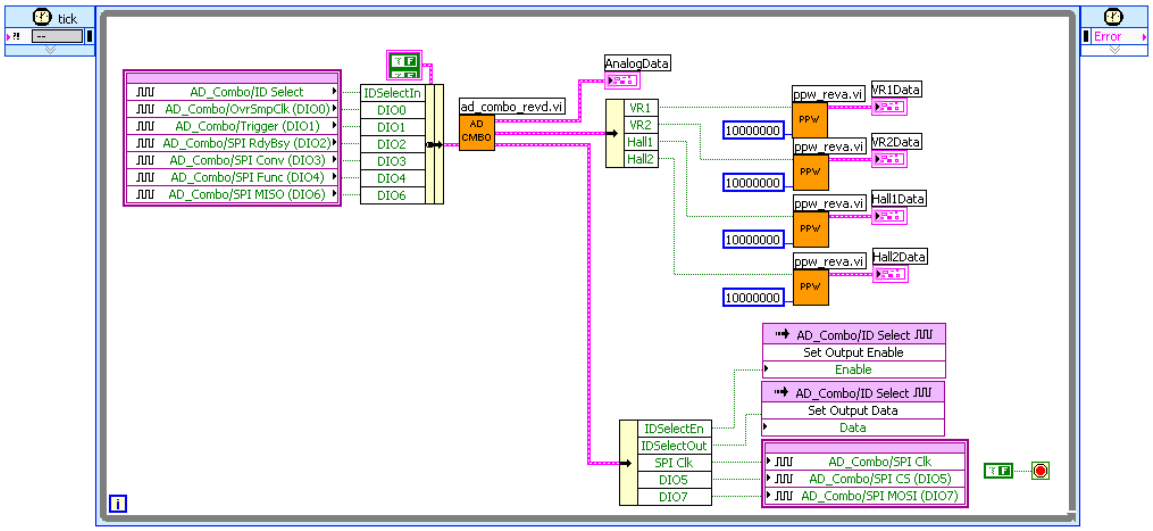


Figure 15. LabVIEW FPGA Block diagram example of ad_combo.vi used as general purpose analog and speed measurement.

Standard Circuit Configuration

The AD Combo module is hardware-configurable. It may be ordered with the default options outlined below or may be custom ordered. Additionally, it may be configured by the user. However, this procedure is only recommended for users highly skilled in circuit board rework due to the small surface mount parts involved.

Standard Analog Configuration

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
1	open	1k	5.6k	200	33V Measurment
2	open	1k	5.6k	200	33V Measurment
3	open	1k	5.6k	200	33V Measurment
4	open	51k	0	500	Active / Pot
5	open	51k	0	500	Active / Pot
6	open	51k	0	500	Active / Pot
7	open	51k	0	500	Active / Pot
8	open	51k	0	500	Active / Pot
9	open	51k	0	500	Active / Pot
10	open	51k	0	500	Active / Pot
11	open	51k	0	500	Active / Pot
12	open	51k	0	500	Active / Pot
13	open	51k	0	500	Active / Pot
14	open	51k	0	500	Active / Pot
15	open	51k	0	500	Active / Pot
16	open	51k	0	500	Active / Pot
17	1k	open	0	500	Thermistor / Switch
18	1k	open	0	500	Thermistor / Switch
19	1k	open	0	500	Thermistor / Switch
20	1k	open	0	500	Thermistor / Switch
21	1k	open	0	500	Thermistor / Switch
22	2.5 Volt (0.2%) Precision Reference				

Standard VR Configuration

Channel	VR Amplitude Voltage
1	60VDC
2	60VDC

Standard Hall Configuration

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
1	4.7k	open	0	150K	Hall, Prox, Switch or TTL
2	4.7k	open	0	150K	Hall, Prox, Switch or TTL

Custom Configuration

For an additional service charge, Drivven will custom configure each analog, VR and Hall channel. Customization can take place during or after module purchase.

It is possible for the customer to configure the channels. All user serviceable parts are on the bottom of the board and their locations are shown in Figure 16. To change the analog or hall circuit configuration, use the resistor-type and channel-number grid headings on the top and sides, respectively, to locate the component you wish to change. The VR Limit resistor can be configured to change the maximum amplitude voltage setting as follows:

Resistance = MaxAmplitude (V) / 0.003 (A)

The VR Adapt location should not be modified.

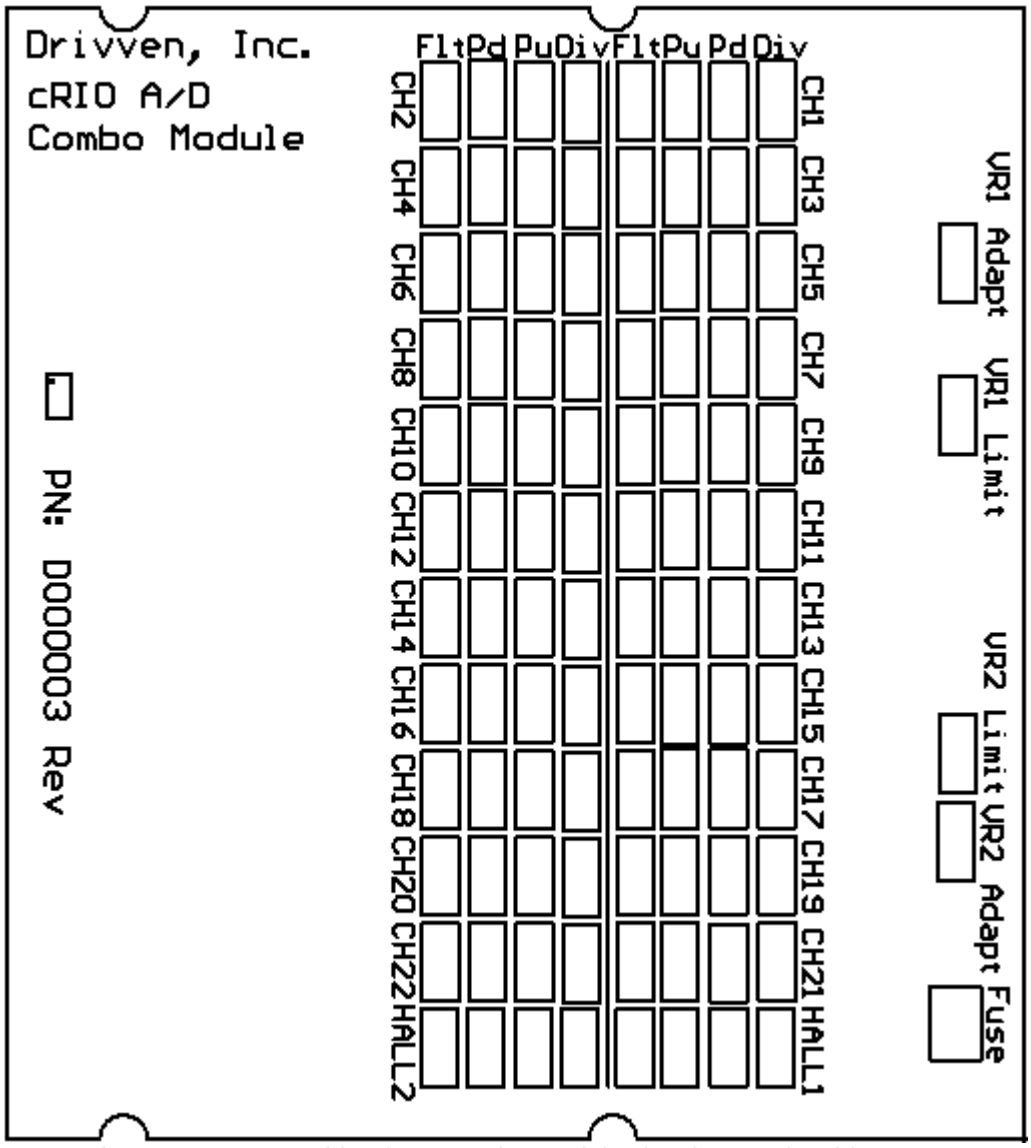


Figure 16. Bottom side of AD Combo module showing serviceable parts.

When requesting a custom configuration, please provide all of the following information.

Customer Business Name	
Contact Name	
Contact Phone	
Contact Email	
Shipping Address	
Unit Serial Number	
Has this unit been modified by the user?	

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
Analog 1					
Analog 2					
Analog 3					
Analog 4					
Analog 5					
Analog 6					
Analog 7					
Analog 8					
Analog 9					
Analog 10					
Analog 11					
Analog 12					
Analog 13					
Analog 14					
Analog 15					
Analog 16					
Analog 17					
Analog 18					
Analog 19					
Analog 20					
Analog 21					
Hall 1					
Hall 2					

Channel	VR Amplitude Voltage
VR 1	
VR 2	

Compliance and Certifications

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Industrial immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Caution: When operating this product, use shielded cables and accessories.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers. For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit `ni.com/environment/weee`.

Battery Replacement and Disposal

Battery Directive This device contains a long-life coin cell battery. If you need to replace it, use the Return Material Authorization (RMA) process or contact an authorized National Instruments service representative. For more information about compliance with the EU Battery Directive 2006/66/EC about Batteries and Accumulators and Waste Batteries and Accumulators, visit `ni.com/environment/batterydirective`.

Ferrite Requirement for EMC Compliance

Install a clamp-on ferrite bead onto both the power supply cable and the signal cable. Power to the module must be off when adding ferrites. Ferrites must be connected to the power cable and the signal cable as close to the module as possible. Placing the ferrite elsewhere on the cable noticeably impairs its effectiveness. Determine the clamp-on ferrite beads to install based on your application. Use the following ferrites or other similar ferrites:
Power cable: Laird 28A0592-0A2 (2 total)
Signal cable: Wurth Electronics 7427154 (2 total)

Management Methods for Controlling Pollution Caused by Electronic Information Products Regulation (China RoHS)

Chinese Customers National Instruments is in compliance with the Chinese policy on the Restriction of Hazardous Substances (RoHS) used in Electronic Information Products. For more information about the National Instruments China RoHS compliance, visit ni.com/environment/rohs_china.

电子信息产品污染控制管理办法（中国RoHS）

中国客户 National Instruments符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于National Instruments中国RoHS合规性信息，请登录ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Physical Specifications and Characteristics

Weight: 145 grams
Maximum Altitude: 2000 m
Operating Temperature: -40° C to 70° C
Maximum Ambient Temperature: 70° C
Operating Humidity: 10% to 90% RH, noncondensing
Pollution Degree: 2
Ingress Protection: IP40
For Indoor Use Only
If you need to clean the module, wipe it with a dry towel

Safety Guidelines

Caution: Do not operate this module in a manner not specified in these operating instructions. Do not exceed the 60VDC rating. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.